IN THE SPECIFICATION:

Please replace the paragraph appearing at page 25, line 11 to page 26, line 2 with the following:

Figure 5 illustrates a block diagram of an example embodiment of a sequence generator configured using a linear feedback shift register or scrambler type implementation. An input 500 connects to a summing unit 504. All arithmetic operations may be performed in a modulo-2 fashion. The summing unit 504 has an output connected to an output line 508 and a delay register 510A. The output of the delay register 510A connects to a multiplier 514A, having a multiplier set to C_1, and to another delay register 510B. The output of delay register 510B connects to N number of other delay registers and multipliers as shown by connections 524 until connecting to a delay register 510C and to a multiplier 514B, set to C_{N-1}. The output of delay register 510C connects to a multiplier 514C, set to C_N. ~~connecting to a delay register 510C and to a multiplier 514B C_{N-1}. The output of delay register 510C connects to a multiplier 514C that has a multiplier C_N.~~ One or more summing junctions 520A, 520B, 520C as shown combine the output from the multipliers. This creates an Nth order generator due to the N memory elements or delay registers 510. This thus generates an output based on the content of the registers, also known as the state of the scrambler. Thus, the total number of different possible states of the generator is 2^N.